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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/766,046	01/28/2004	Gi Jeong Kim	AMKOR-099A	2288

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EXAMINER	
HARRISON, MONICA D	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 09/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/766,046	KIM ET AL.	
	Examiner	Art Unit	
	Monica D. Harrison	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3/21/05 7/12/04 7/9/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Marrs (5,485,037).

1. Regarding claim 1, Marrs discloses a semiconductor package comprising: a heat sink having opposed top and bottom surfaces and defining a peripheral edge (Figure 1A, reference 101); a semiconductor die attached to the top surface of the heat sink (Figure 1A, reference 106); a plurality of leads extending at least partially about the semiconductor die (Figure 1A, reference 107), the semiconductor die being electrically connected to at least one of the leads (Figure 1A, reference 111); at least one first ground lead attached to the top surface of the heat sink between the semiconductor die and the peripheral edge of the heat sink (Figure 1A, reference 102); at least one second ground lead attached to the top surface of the heat sink and protruding beyond the peripheral edge thereof (Figure 1A, reference 102; *opposing side*); a plurality of ground wires conductively collecting the semiconductor die, the first and second ground leads, and the heat sink to each other (Figure 1A, reference 107); and a package body at least partially encapsulating the heat sink, the semiconductor die, the leads, the first and second ground leads, and the ground wires such that at least portions of the second ground lead and the leads are exposed in the package body (Figure 1A, reference 110).

2. Regarding claim 2, Marrs discloses wherein the first ground lead is secured to the top surface of the heat sink by a first insulating layer (Figure 1A, reference 112); and the second ground lead is secured to the top surface of the heat sink by a second insulating layer (Figure 1A, reference 114).

3. Regarding claim 3, Marrs discloses wherein the first and second insulating layers are each fabricated from a polyimide tape (column 6, lines 3-8).

4. Regarding claim 4, Marrs discloses wherein a plurality of first ground leads is attached to the top surface of the heat sink (Figure 1A, reference 107); a plurality of second ground leads is attached to the top surface of the heat sink (Figure 1A, reference 107); the first and second ground leads are segregated into pairs, with the first and second ground leads of each pair being arranged in aligned, spaced relation to each other; and the first and second ground leads of each pair are disposed between a corresponding adjacent pair of the leads (Figure 1A, reference 102).

5. Regarding claim 5, Marrs discloses wherein a plating section is applied to the top surface of the heat sink (Figure 1A, reference 108); the semiconductor die is conductively connected to the plating section by at least one of the ground wires (Figure 1A, reference 102); the first ground lead of each pair is conductively connected td the plating section by at least two of the ground wires; and the second ground lead of each pair is conductively connected to the plating section by at least one of the ground wires (Figure 1A, reference 107).

6. Regarding claim 6, Marrs discloses wherein the plating section includes: a first region which extends between the semiconductor package and the first ground lead of each set, the semiconductor die being conductively connected to the first region; a third region which

extends between the first and second ground leads of each set, the first ground lead being conductively connected to the first and third regions, with the second ground lead being conductively connected to the third region; and at least one second region which extends between and is integrally connected to the first and third regions (Figure 1A, references 108a, 108b, and 108c; column 5, lines 29-40).

7. Regarding claim 7, Marrs discloses a plurality of second regions which extend between the first and third regions thereof (column 5, lines 29-40).

8. Regarding claim 8, Marrs discloses wherein a plating section is applied to the top surface of the heat sink (Figure 1A, reference 108); the semiconductor die is conductively connected to the plating section by at least one of the ground wires (Figure 1A, reference 102); the first ground lead is conductively connected to the plating section by at least two of the ground wires; and the second ground lead is conductively connected to the plating section by at least one of ground wires (Figure 1A, reference 107).

9. Regarding claim 9, Marrs discloses wherein the first and second ground leads are arranged in aligned, spaced relation to each other (Figure 1A, references 102 and 107); and the plating section includes: a first region which extends between the first ground lead and the semiconductor die, the semiconductor die being conductively connected to the first region; a third region which extends between the first and second ground leads, the first ground lead being conductively connected to the first and third regions, with the second ground lead being conductively connected to the third region; and at least one second region which is integrally connected to and extends between the first and third regions (Figure 1A, references 108a, 108b, and 108c; column 5, lines 29-47).

10. Regarding claim 10, Marrs discloses wherein the plating section includes a plurality of second regions which extend between the first and third regions thereof (column 5, lines 29-40).

11. Regarding claim 11, Marrs discloses wherein the first region of the plating section circumvents the semiconductor die (Figure 1A, references 108a, 108b, or 108c).

12. Regarding claim 12, Marrs discloses wherein the bottom surface of the heat sink is exposed in the package body (Figure 1A, reference 101).

13. Regarding claim 13, Marrs discloses wherein the bottom surface of the heat sink is generally planar and is substantially flush with a generally planar exterior surface of the package body (Figure 1A, reference 101).

14. Regarding claim 14, Marrs discloses further comprising a ring extending between the first ground lead and the semiconductor die (abstract-*interconnect ring*).

15. Regarding claim 15, Marrs discloses a semiconductor package comprising: a heat sink having opposed top and bottom surfaces and defining a peripheral edge (Figure 1A, reference 101); a semiconductor die attached to the top surface of the heat sink (Figure 1A, reference 106); at least one first ground lead attached to the top surface of the heat sink in spaced relation to the semiconductor die (Figure 1A, reference 102); at least one second ground lead attached to the top surface of the heat sink in a plurality of ground wires conductively connecting the semiconductor die (Figure 1A, reference 102; *opposing side*), the spaced relation to the first ground lead; first and second ground leads, and the heat sink to each other (Figure 1A); and a package body at least partially encapsulating the heat sink, the semiconductor die, the first and

second ground leads, and the ground wires such that at least a portion of the second ground lead is exposed in the package body (Figure 1A, reference 110).

16. Regarding claim 16, Marrs discloses a plurality of leads extending at least partially about the semiconductor die (Figure 1A, reference 102); the semiconductor die being electrically connected to at least one of the leads (Figure 1A, reference 107).

17. Regarding claim 17, Marrs discloses a plurality of first ground leads is attached to the top surface of the heat sink (Figure 1A, reference 107); a plurality of second ground leads is attached to the top surface of the heat sink (Figure 1A, reference 107); the first and second ground leads are segregated into pairs, with the first and second ground leads of each pair being arranged in aligned, spaced relation to each other; and the first and second ground leads of each pair are disposed between a corresponding adjacent pair of the leads (*bond wires* Figure 1A, reference 107 *are displaced between package leads* Figure 1A, reference 102).

18. Regarding claim 18, Marrs discloses wherein a plating section is applied to the top surface of the heat sink (Figure 1A, reference 108); the semiconductor die is conductively connected to the plating section by at least one of the ground wires (Figure 1A, reference 102); the first ground lead of each pair is conductively connected to the plating section by at least two of the ground wires (Figure 1A, reference 107); and the second ground lead of each pair is conductively connected to the plating section by at least one of the ground wires (Figure 1A, reference 107).

19. Regarding claim 19, Marrs discloses wherein a plating section is applied to the top surface of the heat sink (Figure 1A, reference 108); the semiconductor die is conductively connected to the plating section by at least one of the ground wires (Figure 1A, reference 102);

the first ground lead is conductively connected to the plating section by at least two of the ground wires (Figure 1A, reference 107); and the second ground lead is conductively connected to the plating section by at least one of the ground wires (Figure 1A, reference 107).

20. Regarding claim 20, Marrs discloses wherein the first and second ground leads are arranged in aligned, spaced relation to each other (Figure 1A, reference 107); and the plating section includes (Figure 1A, reference 108): a first region which extends between the first ground lead and the semiconductor die, the semiconductor die being first region (Figure 1A, reference 106), a third region which extends between the first and second ground leads, the first ground lead being conductively connected to the first and third regions, with the second ground lead being conductively connected to the third region; and at least one second region which is integrally connected to and extends between the first and third regions (Figure 1A, references 108a, 108b, and 108c; column 5, lines 29-40).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica D. Harrison whose telephone number is 571-272-1959. The examiner can normally be reached on M-F 7:00am-3:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Monica D. Harrison
AU 2813

mdh
September 23, 2005

DAVID BLUM
PRIMARY EXAMINER